SUBJECT INDEX

Activities sequences 24 (1988)681
Alternating sequential-parallel systems 24 (1988) 95
Application layer protocol 24 (1988)111
Asymmetric invalidation 24 (1988)723
Asynchronous VLSI systems 24 (1988)347
Automatic protocol generation 24 (1988)111
Autonomous mobile robot 24 (1988)411

B-HIVE multicomputer 24 (1988) 79
Backtracking 24 (1988)607
Behavioral testing techniques 24 (1988) 63
Behavioural simulation 24 (1988)213
Binary search algorithm 24 (1988) 95
Boolean equation 24 (1988)767
Branch execution 24 (1988)573
Branch instructions execution 24 (1988)565
Branch target buffer 24 (1988)573
Butterfly network 24 (1988)353
BW-monitor design 24 (1988)717

Cache parameters 24 (1988)541
CAD tools 24 (1988)767
CAE-workstations 24 (1988)541
Chip image 24 (1988) 29
CMOS 24 (1988) 23, 233, 339
CMOS technology 24 (1988)637
Co-processor for unification 24 (1988)607
Communication circuit 24 (1988)103
Communication memory 24 (1988)503
Communication strategy 24 (1988) 11
Communication virtual processor 24 (1988)511
Compiler 24 (1988)471
Computational model 24 (1988)599
Computer architecture 24 (1988)309
Computer audio research laboratory 24 (1988)443
Computer music 24 (1988)443
Computer network 24 (1988)103
Computer networks 24 (1988)197
Computer science 24 (1988)835
Computer vision 24 (1988)403
Concurrent primitives 24 (1988)257
Concurrent program design 24 (1988) 51, 809
Concurrent program flow checking 24 (1988)783
Concurrent system specification 24 (1988)483
Control 24 (1988)681
Controlled reduction model 24 (1988)607
Coprocessor 24 (1988)599
CPU-coprocessor communication and synchronization 24 (1988)695

Data acquisition automation 24 (1988)549
Data searching 24 (1988)655
Database modeling 24 (1988)249
Databases 24 (1988)599
Dataflow 24 (1988)663
Deadline 24 (1988)491
Decision mechanisms 24 (1988)801
Declarative programming 24 (1988)663

Deductive databases 24 (1988)599
DEOS 24 (1988)241
Design for testability 24 (1988)233
Design language 24 (1988) 35
Design methodology 24 (1988) 43
Design process 24 (1988)219
Design specification 24 (1988)219
Design tools 24 (1988) 29
Digital systems design 24 (1988)227
Distributed associative network 24 (1988)613
Distributed computation 24 (1988)491
Distributed control 24 (1988)607
Distributed databases 24 (1988)249
Distributed operating system 24 (1988)169, 179, 187, 519
Distributed programs 24 (1988) 85
Distributed software fault-tolerant real-time systems 24 (1988)801
Distributed systems 24 (1988)511, 731, 793
DSP 24 (1988)325

Education 24 (1988)757
Embedded ASICs 24 (1988)449
Embedded control systems 24 (1988)663
Embedded control systems programming 24 (1988)663
Embedded multiprocessor systems 24 (1988) 85
Embedded systems 24 (1988) 51, 775, 809
Error detection 24 (1988)629
Error retracing 24 (1988)461

Fast Fourier transform 24 (1988)353
Fault diagnosis 24 (1988)527
Fault localization 24 (1988)461
Fault modeling 24 (1988)233
Fault propagation 24 (1988)723
Fault recovery 24 (1988)775
Fault tolerance 24 (1988)519
Fault-tolerant 24 (1988)629
Fifth compiler 24 (1988) 73
Fixed point processor 24 (1988)695
Floating point coprocessor 24 (1988)695
Formal description language 24 (1988)363
Formal description techniques 24 (1988) 51, 809
Function language 24 (1988)227
Functional microprocessor architecture 24 (1988)149
Functional programs 24 (1988)613
Fuzzy C-means algorithm 24 (1988)647
Fuzzy clustering 24 (1988)647

Galileo nets 24 (1988)483
Global fanout correction 24 (1988) 43
Global optimization 24 (1988)339
Grinding machine control system 24 (1988)663

Hardware description languages 24 (1988)219, 371
Hardware realization of systolic algorithms 24 (1988)527
Hardware simulation environment 24 (1988)291
Hexagonal arithmetic array processors 24 (1988)629
Hierarchical design 24 (1988) 29
Hierarchical physical design system 24 (1988)131
High level debugger 24 (1988)153
High level language 24 (1988) 57, 85
HLL directed architecture 24 (1988)701
Hough transform 24 (1988)403
Human interfaces 24 (1988)153
Hypercube architectures 24 (1988)213

IBM-PC 24 (1988)325
Image processing 24 (1988)309
Image registration system 24 (1988)315

Industrial controllers 24 (1988)775
Instruction set processor 24 (1988)149
Interactive programming tool 24 (1988) 73
Interconnection networks 24 (1988)731
Intermodel transformation 24 (1988)249
International banking 24 (1988) 11

Kernel 24 (1988)161
Knowledge based systems 24 (1988)315

Language coprocessor 24 (1988)701
Laser radar 24 (1988)411
Learning 24 (1988)681
Local area networks 24 (1988) 95, 761
Local optimization 24 (1988)339
Logic design 24 (1988) 35
Logic synthesis 24 (1988) 43, 125, 339
LOTOS 24 (1988)483

Matrix equations 24 (1988)681
Memory management unit 24 (1988)709
Message passing 24 (1988)519
Message-passing hardware 24 (1988)503
Microprocessor simulation 24 (1988)149
Micro systems architecture 24 (1988)103
Microcode 24 (1988)371
Microcode compaction 24 (1988) 17
Microprocessor debugging 24 (1988)149
Microprocessor network 24 (1988) 85
Microprocessors 24 (1988)371, 775
Modula-2 24 (1988)761
Multi level design verification system 24 (1988)137
Multi-microprocessor environment 24 (1988)581
Multi-transputer architectures 24 (1988)281
Multi-transputer net 24 (1988)291
Multilevel digital simulation 24 (1988)299
Multilevel system software 24 (1988) 63
Multiple fault diagnosis 24 (1988)731
Multiplication algorithm 24 (1988)637
Multiprocessor 24 (1988)103, 389, 503, 599
Multiprocessor architecture 24 (1988)673
Multiprocessor environment 24 (1988)819
Music experiment 24 (1988)443
Music processing 24 (1988)435
Music publishing 24 (1988)549
Musical instrument simulator and workstation 24 (1988)555

Numerical stability 24 (1988)527

Oberon 24 (1988) 3
Object-oriented program design 24 (1988)257
Object-oriented system 24 (1988)241
Occam 24 (1988)169, 205, 291, 397, 491, 673, 757
Optimization 24 (1988)541
OR-ed dataflow 24 (1988)663

Parallel algorithms 24 (1988)655
Parallel architectures 24 (1988)197
Parallel computer architectures 24 (1988)363
Parallel computing 24 (1988)535
Parallel event administration 24 (1988)687
Parallel neural network simulation 24 (1988)621
Parallel parsing 24 (1988)819
Parallel processing 24 (1988)291, 747
Parallel processing system 24 (1988)511
Parallel programming 24 (1988)757
Parallelism 24 (1988)599
Parallelizing compiler 24 (1988) 79

PCTE 24 (1988)161
Performance 24 (1988)519
Performance evaluation 24 (1988)197
Performance studies 24 (1988)281
Petri net 24 (1988)471
Petri net semantics 24 (1988)267
Petri net models 24 (1988)197
Pipelined architecture 24 (1988)709
Polymorphic-torus architecture 24 (1988)737
Power applications 24 (1988)589
Predicate/transition sets 24 (1988)267
Process structure 24 (1988)187
Process technology 24 (1988) 29
Processor array 24 (1988)655
Processor interconnections 24 (1988)197
Programming paradigms 24 (1988)535
Prolog machine 24 (1988)607
Protocol description 24 (1988)205
Protocol design 24 (1988)483
Prototyping language 24 (1988)471

Quantitative analysis 24 (1988)197

Racah coefficients 24 (1988)535
Reachability analysis 24 (1988)809
Real-time 24 (1988)491, 519, 757
Real-time applicationa 24 (1988)717
Real-time process control and supervision 24 (1988)829
Real-time programming 24 (1988) 73
Real-time speech-synthesis 24 (1988)325
Real-time structured analysis 24 (1988)449
Real-time system design 24 (1988)379
Real-time systems 24 (1988)257, 687
Real-time systems education 24 (1988)835
Real-time data processing 24 (1988)411
Recognition system 24 (1988)425
Reduction machine 24 (1988)389
Relational database system 24 (1988)555
Risc architecture 24 (1988)565
Risc biprocessor architecture 24 (1988)589
Risc for image generation 24 (1988)581
Risc processor 24 (1988)573
Robot-arm control 24 (1988)673
Robotics 24 (1988)419
Robust software design 24 (1988)793

Safety-critical applications 24 (1988)371
Scheduling 24 (1988)681
Self-checking capability 24 (1988)637
Server-oriented systems 24 (1988)179
Simulation 24 (1988)205, 681
Simulation results evaluation 24 (1988)461
Single process multitasking system 24 (1988) 3
Single-chip microcomputers 24 (1988)783
Software development 24 (1988)179
Software engineering environment 24 (1988)161
Software training environment 24 (1988)761
Sparse matrix techniques 24 (1988)621
Specification and verification 24 (1988)371
Speech processing 24 (1988)397
State space modelling 24 (1988)793
Static and dynamic links 24 (1988)281
Stochastic force sensing 24 (1988)419
Strategical level 24 (1988)681
String processor architecture 24 (1988)747
Supercomputing 24 (1988) 17
Symbolic processing 24 (1988)599

Synchronization	24 (1988)187
System behaviour	24 (1988)227
System faults diagnosability	24 (1988)723
System level design	24 (1988)449
System level language	24 (1988) 57
System logic	24 (1988) 29
System programming	24 (1988) 57
System structure	24 (1988)227
System structuring	24 (1988)187
System timing	24 (1988)347
Systems modelling and analysis	24 (1988) 51, 809
Systolic arrays	24 (1988)527
Tactile data	24 (1988)425
Test pattern generation	24 (1988)233
Testability	24 (1988)275
Text and graphics integration	24 (1988)455
Timing correction	24 (1988) 43
Timing correction algorithm	24 (1988)125
Timing verification	24 (1988)125
Topology	24 (1988)275
Transformation rules	24 (1988)397
Transient fault tolerance	24 (1988)775
Translation lookaside buffer	24 (1988)709
Transputer	24 (1988)607
Transputer network	24 (1988) 73, 169, 389
Transputer-based accelerator	24 (1988)299
Transputers	24 (1988)275, 397, 403, 535, 673, 757
UNIX	24 (1988)761
Unlimited vocabulary	24 (1988)325
Validation and verification	24 (1988)809
Vector processing	24 (1988)743
Vectorized superminicomputer	24 (1988)743
Verification	24 (1988)137
VLSI	24 (1988)209
VLSI CAD tools	24 (1988)455
VLSI design	24 (1988)767
VLSI design methodology	24 (1988)371
VLSI implementation	24 (1988)737
VLSI serial multiplier	24 (1988)637
VLSI systolic architecture	24 (1988)647
VLSI-/370 microprocessor	24 (1988) 23, 29, 35, 43, 125, 131, 137
Wisdom	24 (1988)169
Workstations	24 (1988) 3, 11
WP-calculus	24 (1988)491

AUTHOR INDEX

Adamson, K., Donnan, G. and Black, N.D., Simple Transformation Rules in the Application of Transputers to the Physiological Processing of Speech 24 (1988)397
Agrawal, D.P. and Mauney, J., Structure of a Parallelizing Compiler for the B-HIVE Multicomputer 24 (1988) 79
Allerton, D.J., see Anido, M.L. 24 (1988)581
Ancona, M., Bottino, T., Clematis, A., Dodero, G., Gianuzzi, V., Pareto, L., Pronzato, M. and Repetti, A., LINDA: An Allocator for Embedded Multiprocessor Systems 24 (1988) 85
Ancona, M., Clematis, A. and Gianuzzi, V., Two Language Levels For System Programming 24 (1988) 57
Anger, H., see Hahn, W. 24 (1988)291
Anido, M.L., Allerton, D.J. and Zaluska, E.J., The Architecture of RIG: A RISC for Image Generation in a Multi-Microprocessor Environment 24 (1988)581
Antipa, V., see Krolak, S.T. 24 (1988)241
Antola, A., Evaluation of Complexity for Different Layouts of Butterfly Networks 24 (1988)353
Auer, A., Kemppainen, P., Okkonen, A. and Seppanen, V., Automated Code Generation of Embedded Real-Time Systems 24 (1988) 51

Barbosa, V.C. and Franca, F.M.G., Specification of a Communication Virtual Processor for Parallel Processing Systems 24 (1988)511
Bemmerl, T. and Bonk, T., Optimizing Cache Parameters using CAE Workstations 24 (1988)541
Bemmerl, T., Erl, N. and Hansen, O., Menu and Graphic Driven Human Interfaces for High Level Debuggers 24 (1988)153
Berbers, Y. and Verbaeten, P., Design of the Hermix Distributed Operating System: Structural Aspects 24 (1988)187
Billingsley, J., see Luk, B.L. 24 (1988)419
Bisio, G.M., see Curatelli, F. 24 (1988)213
Black, N.D., see Adamson, K. 24 (1988)397
Bonk, T., see Bemmerl, T. 24 (1988)541
Borghero, G., see Curatelli, F. 24 (1988)213
Bottino, T., see Ancona, M. 24 (1988) 85
Boudillet, O., Winter, S.C. and Wilson, D.R., The Implementation of a Functional Machine on a Transputer Network 24 (1988)389
Breveglieri, L., Design and Implementation of a VLSI Serial Multiplier for Fixed Point Numbers with Self-Checking capability 24 (1988)637
Brezany, P., Parallel Parsing in a Multiprocessor Environment 24 (1988)819
Brown, B.M., see Clarke, A.T. 24 (1988)549
Burki, M., see Hersch, R.D. 24 (1988)503
Buschke, R. and Lagemann, K., Error Retracing and Fault Localization Techniques within SIMUEVA, a System for Evaluation of Simulation Results 24 (1988)461

Carpenter, G.F., see Holding, D.J. 24 (1988)801
Carpenter, G.F., State Space Modelling in the Design of Robust Software for Distributed Systems: A Case Study 24 (1988)793
Cegrell, T., see Sandberg, U. 24 (1988)829
Chalmers, A., OCCAM - The Language for Educating Future Parallel Programmers? 24 (1988)757
Christodoulakis, D.N., Petri Net Semantics of Smalltalk-80 24 (1988)267
Clarke, A.T., Brown, B.M. and Thorne, M.P., Using a Micro to Automate Data Acquisition in Music Publishing 24 (1988)549
Clematis, A., see Ancona, M. 24 (1988) 57

Clematis, A., see Ancona, M. 24 (1988) 85
Cohen, E.J., Marko, R.A. and Levy, J., Integrating an On-Chip MMU into a Highly Pipelined Architecture 24 (1988)709
Collier, M., A Software Training Environment for Electronic Engineers using UNIX, Modula-2 and a Local Area Network 24 (1988)761
Comerford, P.J. and Eaglestone, B.M., Bradford Musical Instrument Simulator and Workstation 24 (1988)555
Cook, J. and Gilbert, J., Parallel Neural Network Simulation Using Sparse Matrix Techniques 24 (1988)621
Cortadella, J. and Jove, T., Designing a Branch Target Buffer for Executing Branches with Zero Time Cost in a RISC Processor 24 (1988)573
Cortadella, J., see Gonzalez, A. 24 (1988)565
Couprie, M., see Gonzalez-Rubio, R. 24 (1988)599
Crookes, D., see Scott, N.S. 24 (1988)535
Curatelli, F., Bisio, G.M., Borghero, G. and Di Zitti, E., A Behavioural Simulator and Its Use for the Validation of Hypercube Architectures 24 (1988)213

Dang, M., Diot, C., Sabouni, I. and Sponga, L., Specific Data Structure Intended for the Implementation of High Level ISO Standards: Associated Algorithms and Dedicated Hardware 24 (1988)103
Das, P.K. and Fay, D.Q.M., Performance Studies of Multi-Transputer Architectures with Static and Dynamic Links 24 (1988)281
De Blasi, M., Gentile, A., Lopez, G. and Franco, A., Parallel Backtracking Prolog Engine 24 (1988)607
De Man, J.A., Designing Digital Systems with a Function Language 24 (1988)227
Debaere, E.H., A Language Coprocessor as an HLL Directed Architecture 24 (1988)701
Decuypere, H.J.M., see Hellemans, P.M.J. 24 (1988)111
Devesa, N., Goncalves, G., Lecouffe, M.-P. and Toursel, B., A Controlled Reduction Model of Functional Programs on a Distributed Associative Network 24 (1988)613
Di Zitti, E., see Curatelli, F. 24 (1988)213
Diot, C., see Dang, M. 24 (1988)103
Dirkx, E. and Tiberghien, J., An Animated Simulation Environment for Microprocessors 24 (1988)149
Dirkx, E., see Van der Jeugt, G. 24 (1988)205
Distante, F. and Sciuto, D., Behavioral Testing of Multilevel System Software 24 (1988) 63
Doallo, R., see Zapata, E.L. 24 (1988)647
Dodero, G., see Ancona, M. 24 (1988) 85
Donnan, G., see Adamson, K. 24 (1988)397
Dumont, A., Gilson, E. and Trullemans, C., BRISC: A RISC Biprocessor Architecture Dedicated to Power Applications 24 (1988)589

Eaglestone, B.M., see Comerford, P.J. 24 (1988)555
Eghtesadi, S., see Sandler, M.B. 24 (1988)403
Eichenseher, I., Ungerer, T. and Zehendner, E., CADL - A Formal Description Language for Parallel Computer Architectures 24 (1988)363
Erl, N., see Bemmerl, T. 24 (1988)153

Fay, D.Q.M., see Das, P.K. 24 (1988)281
Fernandes, P., see Navaux, P. 24 (1988)197
Fernin, P., Winter, S.C., Wilson, D.R. and Reignier, H., Implementation of an Intelligent SAR Image Registration System 24 (1988)315
Fisher, J.A., Microprogramming, Microprocessing and Supercomputing 24 (1988) 17
Fox, A., see Loewenstein, P. 24 (1988)767
Fox, A., Spracklen, T. and Jolly, C.P., Logic Synthesis with Constraints 24 (1988)339
Franca, F.M.G., see Barbosa, V.C. 24 (1988)511
Franco, A., see De Blasi, M. 24 (1988)607

Gentile, A., see De Blasi, M. 24 (1988)607
Gerst, H., Verification of the VLSI-/370 Microprocessor 24 (1988)137
Gianuzzi, V., see Ancona, M. 24 (1988) 57
Gianuzzi, V., see Ancona, M. 24 (1988) 85
Gilbert, J., see Cook, J. 24 (1988)621
Gilson, E., see Dumont, A. 24 (1988)589
Glowacz, C., see Matthaus, C. 24 (1988)233
Goncalves, G., see Devesa, N. 24 (1988)613
Gonzalez, A., Llaberia, J.M. and Cortadella, J., A Mechanism for Reducing the Cost of Branches in RISC Architectures 24 (1988)565
Gonzalez-Rubio, R. and Couprie, M., DDC: Delta Driven Computer, and mSyC: Microprogrammable Symbolic Coprocessor 24 (1988)599
Gruhn, V. and Hallmann, M., A Petri Net Based Compiler for the Prototyping Language RELOS 24 (1988)471
Guiheux, H., Mardapittas, C., Wilson, D.R. and Winter, S.C., A Model Based Recognition System for Tactile Data 24 (1988)425
Gunhildsbu, O.M., see Knoppers, P. 24 (1988)275

Hagerer, A., see Hahn, W. 24 (1988)291
Hahn, W., Anger, H., Hagerer, A. and Schuster, B., A Multi-Transputer-Net as a Hardware Simulation Environment 24 (1988)291
Halang, W.A., Parallel Administration of Events in Real-Time Systems 24 (1988)687
Hallmann, M., see Gruhn, V. 24 (1988)471
Hansen, O., see Bemmerl, T. 24 (1988)153
Haus, G., Music Processing at L.I.M. 24 (1988)435
Heinkele, S., Timing Verification for the VLSI-/370 Microprocessor 24 (1988)125
Hellemans, P.M.J. and Decuypere, H.J.M., Automatic Protocol Generation Based on X.409 Specifications 24 (1988)111
Hersch, R.D., Maddaleno, F., Nicks, C. and Burki, M., The Video-Ram Multiprocessor Architecture 24 (1988)503
Hill, M.R., see Holding, D.J. 24 (1988)801
Hinkel, R., Knieriemen, T. and von Puttkamer, E., A Rotating Laser Range Finder and Attached Data Interpretation for Use in an Autonomous Mobile Robot 24 (1988)411
Holding, D.J., Hill, M.R. and Carpenter, G.F., The Design of Distributed, Software Fault Tolerant, Real-Time Systems Incorporating Decision Mechanisms 24 (1988)801
Houghton, A.D. and Seed, N.L., A Computer Architecture for Real Time Image Processing Using VLSI 24 (1988)309
Huang, K., Diagnosability of System Faults with Propagation under Asymmetric Invalidation 24 (1988)723
Hubner, U., see Matthaus, C. 24 (1988)233
Huschke, H., Communications Strategies in International Banking 24 (1988) 11

Ismail, M.A., see Zapata, E.L. 24 (1988)647

Jansen, P.G., see Smit, G.J.M. 24 (1988)519
Jockovic, M., An Application of Petri-Nets in the Control System of the FTC 24 (1988)681
Jolly, C.P., see Fox, A. 24 (1988)339
Jove, T., see Cortadella, J. 24 (1988)573
Joyce, J.J., Formal Specification and Verification of Microprocessor Systems 24 (1988)371
Juntunen, T., Kivela, J., Reinikka, A., Sipola, M., Soininen, J.-P., Tiensyrja, K. and Tikkanen, T., Real-Time Structured Analysis in System Level Design of Embedded ASICs 24 (1988)449

Kanopoulos, N. and Marinos, P., Design of a Bus-Monitor for Real-Time Applications 24 (1988)717
Katbab, A., A Multiprocessor Architecture for Robot-Arm Control 24 (1988)673
Kemppainen, P., see Auer, A. 24 (1988) 51
Kick, B., Logic Synthesis in the Design of the VLSI-/370 Microprocessor 24 (1988) 43
Kilpatrick, P.L., see Scott, N.S. 24 (1988)535

Kivela, J., see Juntunen, T. 24 (1988)449
Knieriemen, T., see Hinkel, R. 24 (1988)411
Knoppers, P., Van de Goor, A.J., Gunhildsbu, O.M. and Stravers, P., Transputer Network with Flexible Topology 24 (1988)275
Krikelis, A. and Lea, R.M., An Associative String Processor Architecture for Parallel Processing Applications 24 (1988)747
Krolak, S.T. and Antipa, V., DEOS - A Dynamically Extendible Object-Oriented System 24 (1988)241
Kruger-Sprengel, B., see Matthaus, C. 24 (1988)233
Kuckendahl, P., see Rauscher, R. 24 (1988)527
Kurmann, H., Lent, B. and Marti, R., Declarative Programming of the Embedded Control Systems Based on OR-ed Dataflow Operational Principle 24 (1988)663

Lagemann, K., see Buschke, R. 24 (1988)461
Lea, R.M., see Krikelis, A. 24 (1988)747
Lecouffe, M.-P., see Devesa, N. 24 (1988)613
Lent, B., see Kurmann, H. 24 (1988)663
Leon, G. and Marchena, S., Formal Conversion Between LOTOS Specification and Galileo Nets 24 (1988)483
Levy, J., see Cohen, E.J. 24 (1988)709
Li, H., see Maresca, M 24 (1988)737
Llaberia, J.M., see Gonzalez, A. 24 (1988)565
Loewenstein, P. and Fox, A., Closing the Semantic Gap 24 (1988)767
Lopez, G., see De Blasi, M. 24 (1988)607
Luk, B.L., Naghdy, F. and Billingsley, J., Stochastic Force Sensing Application in Robotics 24 (1988)419

Maddaleno, F., see Hersch, R.D. 24 (1988)503
Marchena, S., see Leon, G. 24 (1988)483
Mardapittas, C., see Guiheux, H. 24 (1988)425
Maresca, M. and Li, H., A VLSI Implementation of Polymorphic-Torus Architecture 24 (1988)737
Marinos, L. and Papazoglou, M.P., Enhancing Intermodel Transformations in a Distributed Object Oriented Database System 24 (1988)249
Marinos, P., see Kanopoulos, N. 24 (1988)717
Marko, R.A., see Cohen, E.J. 24 (1988)709
Marti, R., see Kurmann, H. 24 (1988)663
Matthaus, C., Kruger-Sprengel, B., Glowacz, C., Hubner, U. and Vierhaus, H.T., CMOS Fault Modeling, Test Generation and Design for Testability 24 (1988)233
Mauney, J., see Agrawal, D.P. 24 (1988) 79
Mayer-Lindenberg, F., Practical Multiprocessor and Realtime Programming in the Fifth Programming Environment 24 (1988) 73
Milligan, L.C., see Scott, N.S. 24 (1988)535
Moons, H. and Verbaeten, P., Software Development in Server-Oriented Systems: The HERMIX Approach 24 (1988)179
Morrow, P.J., see Scott, N.S. 24 (1988)535
Murray, K.A. and Wellings, A.J., Issues in the Design and Implementation of a Distributed Operating System for a Network of Transputers 24 (1988)169

Naghdy, F., see Luk, B.L. 24 (1988)419
Nanninga, G.J., see Van de Goor, A.J. 24 (1988)325
Navaux, P., Fernandes, P. and Tazza, M., SARA: A Processor Interconnection Performance Analysis Tool 24 (1988)197
Nicks, C., see Hersch, R.D. 24 (1988)503

Okkonen, A., see Auer, A. 24 (1988) 51
Oklobdzija, V.G., Issues in CPU-Coprocessor Communication and Synchronization 24 (1988)695

Page, R.M.R., see Reddaway, S.F. 24 (1988)655
Painke, H., VLSI-/370 Microprocessor Overview 24 (1988) 23
Papazoglou, M.P., see Marinos, L. 24 (1988)249
Pareto, L., see Ancona, M. 24 (1988) 85
Payer, M., see Rauscher, R. 24 (1988)527
Pedersen, B.G., Design of Real-Time Systems - A Method and a Tool 24 (1988)379

Peng, Z., Let's Design Asynchronous VLSI Systems 24 (1988)347
Piuri, V., Fault-Tolerant Hexagonal Arithmetic Array Processors 24 (1988)629
Plessmann, K.W. and Tassakos, L., Concurrent, Object-Oriented Program Design in Real-Time Systems 24 (1988)257
Preece, C., see Wingate, G.A.S. 24 (1988)775
Pronzato, M., see Ancona, M. 24 (1988) 85

Rammig, F.J., Schrewe, M. and Vorloeper, G., A Transputer-Based Accelerator for Multilevel Digital Simulation 24 (1988)299
Raud, R., A Language Environment for Asic Design 24 (1988)219
Rauscher, R., Kuckendahl, P. and Payer, M., A System for Estimation of Numerical Stability for Matrix Operations in Systolic Arrays 24 (1988)527
Reddaway, S.F. and Page, R.M.R., High Speed Data Searching with a Processor Array 24 (1988)655
Reignier, H., see Fernin, P. 24 (1988)315
Reinikka, A., see Juntunen, T. 24 (1988)449
Repetti, A., see Ancona, M. 24 (1988) 85
Rivera, F.F., see Zapata, E.L. 24 (1988)647
Roesner, W., The Logic Design Language and Verification Environment for the VLSI-/370 24 (1988) 35

Sabouni, I., see Dang, M. 24 (1988)103
Saeter, T., Software Techniques for Integrating Text and Graphics in VLSI CAD Tools 24 (1988)455
Sandberg, U. and Cegrell, T., Computer Systems for Real-Time Process Control and Supervision - A Framework for Education Based on a Systems Engineering Approach 24 (1988)829
Sandler, M.B. and Eghtesadi, S., Transputer Based Implementations of the Hough Transform for Computer Vision 24 (1988)403
Schettler, H., VLSI-/370 Microprocessor Chip Technology 24 (1988) 29
Schrewe, M., see Rammig, F.J. 24 (1988)299
Schulz, U., Hierarchical Physical Design System for VLSI-/370 Microprocessor 24 (1988)131
Schuster, B., see Hahn, W. 24 (1988)291
Sciuto, D., see Distante, F. 24 (1988) 63
Scott, N.S., Waring, L.C., Milligan, P., Crookes, D., Kilpatrick, P.L. and Morrow, P.J., A Comparison of Programming Paradigms for the Parallel Computation of Racah Coefficients: An Application of Transputers to Computational Atomic Physics 24 (1988)535
Seed, N.L., see Houghton, A.D. 24 (1988)309
Seppanen, V., see Auer, A. 24 (1988) 51
Shi-Sheng, Y., see Shi-Yao, J. 24 (1988)743
Shi-Yao, J., Shuan, Z. and Shi-Sheng, Y., A Vectorized Superminicomputer: VAX-11/780 with Vector Processing 24 (1988)743
Shuan, Z., see Shi-Yao, J. 24 (1988)743
Sipola, M., see Juntunen, T. 24 (1988)449
Smit, G.J.M. and Jansen, P.G., The Communication Processor of TUMULT-64 24 (1988)519
Soininen, J.-P., see Juntunen, T. 24 (1988)449
Sosnowski, J., Concurrent Checking of Program Flow Using Single-Chip Microcomputers 24 (1988)783
Sponga, L., see Dang, M. 24 (1988)103
Spracklen, T., see Fox, A. 24 (1988)339
Stravers, P., see Knoppers, P. 24 (1988)275

Tassakos, L., see Plessmann, K.W. 24 (1988)257
Tazza, M., see Navaux, P. 24 (1988)197
Terenzi, F., The Computer Audio Research Laboratory at the Center for Music Experiment and Related Research 24 (1988)443
Thorne, M.P., see Clarke, A.T. 24 (1988)549
Tiberghien, J., see Dirkx, E. 24 (1988)149
Tiberghien, J., see Van der Jeugt, G. 24 (1988)205
Tiensyrja, K., see Juntunen, T. 24 (1988)449
Tikkanen, T., see Juntunen, T. 24 (1988)449
Toursel, B., see Devesa, N. 24 (1988)613
Trullemans, C., see Dumont, A. 24 (1988)589

Tyszer, J., Multiple Fault Diagnosis for Interconnection Networks for Distributed Systems 24 (1988)731

Ungerer, T., see Eichenseher, I. 24 (1988)363

Valmari, A., PC-Rimst - A Tool for Validating Concurrent Program Designs 24 (1988)809
Van de Goor, A.J. and Nanninga, G.J., Speech Synthesis System with Unlimited Vocabulary for the Dutch Language 24 (1988)325
Van de Goor, A.J., see Knoppers, P. 24 (1988)275
Van der Jeugt, G., Dirkx, E. and Tiberghien J., Protocol Description and Simulation in the OCCAM Programming Language 24 (1988)205
Verbaeten, P., see Berbers, Y. 24 (1988)187
Verbaeten, P., see Moons, H. 24 (1988)179
Verrall, M., PCTE - The Kernel of Software Engineering Environments 24 (1988)161
Vierhaus, H.T., see Matthaus, C. 24 (1988)233
Von Puttkamer, E., see Hinkel, R. 24 (1988)411
Vorloeper, G., see Rammig, F.J. 24 (1988)299

Wallach, Y. and Yaprak, E., Use of Local-Area Networks as Alternating Sequential-Parallel Systems 24 (1988) 95
Waring, L.C., see Scott, N.S. 24 (1988)535
Wellings, A.J., see Murray, K.A. 24 (1988)169
Wilson, D.R., see Boudillet, O. 24 (1988)389
Wilson, D.R., see Fernin, P. 24 (1988)315
Wilson, D.R., see Guiheux, H. 24 (1988)425
Wingate, G.A.S. and Preece, C., Transient Fault Recovery Assessment in 8 and 16 Bit Microprocessor Based Controllers in Embedded Systems 24 (1988)775
Winter, S.C., see Boudillet, O. 24 (1988)389
Winter, S.C., see Fernin, P. 24 (1988)315
Winter, S.C., see Guiheux, H. 24 (1988)425
Wirth, N., Oberon: A System for Workstations 24 (1988) 3

Yaprak, E., see Wallach, Y. 24 (1988) 95

Zaluska, E.J., see Anido, M.L. 24 (1988)581
Zapata, E.L., Doallo, R., Rivera, F.F. and Ismail, M.A., A VLSI Systolic Architecture for Fuzzy Clustering 24 (1988)647
Zedan, H., On the Analysis of Occam Real-Time Distributed Computations 24 (1988)491
Zehendner, E., see Eichenseher, I. 24 (1988)363
Zobel, R.N., Real-Time Systems Education in Computer Science at Manchester University 24 (1988)835